AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Withdrawn) A data driving apparatus for a liquid crystal display device, comprising:

a shift register part sequentially shifting an input source start pulse in accordance with an input source shift clock to generate a sampling signal;

a latch part sequentially latching a plurality of digital pixel data in response to the sampling signal from the shift register part;

a first multiplexer part performing a time-division on the digital pixel data from the latch part, the digital pixel data sequentially being outputted to positive and negative paths by unit of adjacent digital pixel data;

a digital-analog converter part including:

a positive digital-analog converter converting one digital pixel data of the adjacent digital pixel data inputted to the positive path into a positive pixel signal; and

a negative digital-analog converter converting the other digital pixel data of the adjacent digital pixel data inputted to the negative path into a negative pixel signal;

a demultiplexer part supplying the positive pixel signal from the positive digital-analog converter and the negative pixel signal from the negative digital-analog converter to corresponding output channels during the first half of a horizontal period and during the second half of the horizontal period; and

an output part including:

a sampling part sampling the positive pixel signals and the negative pixel signals from the demultiplexer;

a holding part holding the sampled pixel signals from the sampling part; and

an output buffer part for buffering the held pixel signals from the holding part, and

a second multiplexer part for simultaneously outputting the pixel signals from the output buffer part in response to a source output enable signal during the next horizontal period following the horizontal period,

wherein the first multiplexer and the demultiplexer part are controlled by an ODD/EVEN signal which performs the time-division for a horizontal period and a polarity control signal,

wherein the digital-analog converter part comprises:

a third multiplexer part selecting one of the positive and the negative pixel signals in accordance with a source output enable signal and providing the selected pixel signal to the demultiplexer part.

2-7. (Cancelled)

8. (Withdrawn) The apparatus according to claim 1, wherein the sampling part is controlled by an ODD/EVEN signal which performs the time-division on a horizontal period.

9. (Currently Amended) A data driving apparatus for a liquid crystal display device, comprising:

a shift register sequentially shifting an input source start pulse in accordance with an input source shift clock to generate a sampling signal;

a latch part sequentially latching a plurality of digital pixel data in response to the sampling signal from the shift register part;

a multiplexer part performing a time-division on the digital pixel data for a plurality of data lines for a first horizontal period using a polarity control signal and an even/odd signal, the digital pixel data sequentially being outputted to positive and negative paths by unit of adjacent digital pixel data;

a level shifter part raising a voltage of the time-divided pixel data directly supplied from the positive and negative paths of the multiplexer part;

a digital-analog converter part including:

a positive digital-analog converter converting one digital pixel data of the adjacent digital pixel data inputted to the positive path into a positive pixel signal; and

a negative digital-analog converter converting the other digital pixel data of the adjacent digital pixel data inputted to the negative path into a negative pixel signal;

a demultiplexer part providing the positive pixel signal from the positive digital-analog converter and the negative pixel signal received from the digital-analog converter to output channels of the demultiplexer corresponding to the data lines, during the first half of the first horizontal period and during the second half of the first horizontal period; and

an output part including:

a sampling part sampling the positive pixel signals and the negative pixel signals from the demultiplexer;

a holding part holding the sampled pixel signals provided through the sampling part during the previous horizontal period of the first horizontal period; and

a discharging part connected between output buffers and the data lines and simultaneously outputting the pixel signals held in the holding part for the first horizontal period to corresponding data lines for an enable period of a source output enable signal and outputting a

common voltage Vcom to the corresponding data lines for a disable period of the source output enable signal,

wherein the sampling part and the holding part sample and hold the pixel signals supplied for the next horizontal period through the channel different from that of the pixel signal supplied for the first horizontal period,

wherein the common voltage Vcom is the voltage for driving a liquid crystal cell.

10. (Cancelled)

11. (Previously Presented) The apparatus according to claim 9, wherein the multiplexer part comprises:

a plurality of positive path switches coupled to input channels for the pixel data and commonly connected to the positive polarity output channel; and

a plurality of negative path switches coupled to the input channels for the pixel data, connected to the positive path switches in parallel, and commonly connected to negative polarity output channel.

12. (Previously Presented) The apparatus according to claim 9, wherein the demultiplexer part comprises:

a plurality of positive path switches forming a plurality of different positive paths corresponding to the data lines, and commonly connected to a positive digital-analog converter; and

a plurality of negative path switches forming a plurality of different negative paths, commonly connected to a negative digital-analog converter, wherein the negative path switches are connected to the positive path switches in parallel.

13. (Cancelled)

14. (Cancelled)

15. (Previously Presented) The apparatus according to claim 9, wherein the sampling part has a second demultiplexer part comprising;

a plurality of the positive path switches forming a plurality of different positive paths and connected to the output channels of the demultiplexer part; and

a plurality of negative path switches forming a plurality of different negative paths and connected to the output channels of the demultiplexer part.

16. (Previously Presented) The apparatus according to claim 15, wherein the holding part comprises:

positive path capacitors charging and holding the positive pixel signals from the positive path switches of the second demultiplexer part; and

negative path capacitors charging and holding the negative pixel signals from the negative path switches of the second demultiplexer part.

17. (Previously Presented) The apparatus according to claim 16, wherein the discharging part comprises:

a second multiplexer part having:

a plurality of positive path switches connected to the positive path switches of the second demultiplexer through the holding part and connected to the data lines; and

a plurality of the negative path switches connected to the negative switches of the second demultiplexer through the holding part and connected to the data lines.

18. (Previously Presented) The apparatus according to claim 17, wherein the multiplexer, the demultiplexer, and the second demultiplexer are controlled by a first control

signal through an input polarity control signal and an ODD/EVEN signal performing the time-division on the first horizontal period.

19. (Previously Presented) The apparatus according to claim 18, wherein the ODD/EVEN signal performs the time-division on an enable period determined by a source output enable signal for the first horizontal period.

20. (Original) The apparatus according to claim 18, wherein the ODD/EVEN signal further performs the time-division on a disable period of the source output enable signal.

21. (Original) The apparatus according to claim 20, wherein the multiplexer part, the demultiplexer part, and the second demultiplexer part recharge the holding part with the pixel signals for the disable period, wherein the pixel signals are generated for a previous enable period.

22. (Original) The apparatus according to claim 21, wherein the source output enable signal is generated by increasing the disable period of an external reference source output enable signal in order to secure a recharging period of the holding part.

23. (Previously Presented) The apparatus according to claim 18, the second multiplexer part is controlled by a second control signal that is phase-inversed with respect to the first control signal.

24. (Previously Presented) The apparatus according to claim 18, further comprising an output buffer part buffering the pixel signals discharged from the holding part to the discharging part.

25. (Original) The apparatus according to claim 24, wherein the output buffer part comprises:

a plurality of positive path output buffers connected between the positive path capacitors of the holding part and the positive path switches of the second multiplexer part; and

a plurality of negative path output buffers connected between the negative path capacitors of the holding part and the negative path switches of the second multiplexer part.

26. (Original) The apparatus according to claim 17, further comprising an output buffer part buffering the pixel signal supplied through the output channels of the second multiplexer part and supplying the pixel signals to each of the data lines.

27. (Original) The apparatus according to claim 26, the output buffer part comprises:

a plurality of output buffers connected between the output channels of the second multiplexer part and the data lines.

28. (Cancelled)

29. (Original) The apparatus according to claim 17, further comprising a third multiplexer part supplying the pixel signals from the output part to the corresponding data lines for the enable period of the source output enable signal and commonly supplying a reference voltage of the liquid crystal cells to the corresponding data lines for the disable period of the source output enable signal.

30. (Currently Amended) A data driving method for a liquid crystal display device, comprising:

performing a time-division on a plurality of digital pixel data for a first horizontal period using a polarity control signal and an even/odd signal, the digital pixel data sequentially being outputted to positive and negative paths by unit of adjacent digital pixel data;

raising a voltage of the time-divided pixel data directly supplied from the positive and negative paths using a level shifter;

converting one digital pixel data of the adjacent digital pixel data inputted to the positive path into a positive pixel signal and converting the other digital pixel data of the adjacent digital pixel data inputted to the negative path into a negative pixel signal;

supplying the positive pixel signal and the negative pixel signal to corresponding output channels;

sampling and holding the positive pixel signals and the negative pixel signals during the previous horizontal period of the first horizontal period; and

simultaneously outputting the held pixel signals to corresponding data lines for an enable period of an input source output enable signal of a second horizontal period and outputting a common voltage Vcom to the corresponding data lines for a disable period of the input source output enable signal of the second horizontal period,

wherein the sampling the pixel signals is controlled by an ODD/EVEN signal performing a time-division on a horizontal period,

wherein the common voltage Vcom is the voltage for driving a liquid crystal cell.

31.-47 (Cancelled)